REMARKS

Claims 1-24 are pending in the case. Claims 14-19 and 24 are allowed. Claims 1, 2, 10-13 and 20-22 are rejected. Claims 3-9 are objected to as being dependent upon a rejected base claim but are allowable if rewritten in independent form. Claim 23 is objected to due to informalities but is otherwise allowable. In the present submission, claims 1, 9, 10, 20 and 23 have been amended. Applicant has also amended the specification to correct a typographical error. Reconsideration is respectfully requested.

Claim Objections

Claims 9, 10 and 23 are objected to due to various informalities. In the present submission, claims 9, 10 and 23 have been amended to correct the typographical errors in the claims. Withdrawal of the claim objections as to claims 9, 10 and 23 is respectfully requested.

§112 Rejection

Claims 20-22 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. In the present submission, claim 20 has been amended to recite "a second interface circuit between said interface circuit and said frame buffer." The second interface circuit is now distinguished from the interface circuit recited in claim 14. Claim 20 therefore meets the requirement of §112 and withdrawal of the §112 rejection of claims 20-22 is respectfully requested. The Examiner has indicated that claims 20-22 would be allowable when the §112 rejection is removed.

§103 Rejection

Claims 1-2 and 10-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamashita et al. (U.S. Patent No. 6, 101,271; hereinafter "Yamashita") in view of Post (U.S. Patent No. 7,209,168). The Examiner contends that Figure 1 and related description of Yamashita disclose every limitations of claim 1 except for the two-dimensional array of pixel elements. The Examiner then cites Post for disclosing the two-dimensional array of pixel elements. The Examiner takes official notices for the claim limitations in claims 2, 10 and 11. Applicant respectfully traverses the rejection.

Yamashita discloses a gradation correction device in Figure 1 and related description (col. 4, ln. 42, to col. 5, ln. 57) for "visually adjusts image brightness without changing the dynamic range". The gradation correction device in Figure 1 of Yamashita includes a luminance signal conversion means 1 which generates a luminance signal Y from the RGB video input signals, a correction coefficient calculation means 2 to calculate the correction value K to be applied to the RGB signals at multipliers 3, 4 and 5. A setting means 6 sets the characteristics of the gradation conversion. Yamashita further describes that the correction coefficient calculation means 2 can be implemented as a ROM table (col. 6, ln. 9-17).

Claim 1

Claim 1, as amended, recites:

> 1. A system-on-chip imaging system, comprising:
> an image sensor comprising a two-dimensional array of pixel elements, said image sensor providing pixel data representing an image of a scene;
> a data memory, in communication with said image sensor, for storing pixel codewords, **some of said pixel codewords being indicative of said pixel data and some of said pixel codewords having assigned values representing one or more image processing functions**;
> a programmable lookup table, in communication with said data memory, for providing LUT codewords as output data, said programmable lookup table including a plurality of entries, each entry storing a LUT codeword and each entry being indexed by a respective pixel codeword to provide said stored LUT codeword as said output data; and
> **a processing unit**, in communication with said data memory and said lookup table, for receiving LUT codewords from said lookup table and generating output image data and **for updating said entries of said programmable lookup table to program one or more image processing functions in said programmable lookup table**,
> wherein a first pixel codeword stored in said data memory is used to index said lookup table for causing said lookup table to provide a respective LUT codeword to said processing unit, **said LUT codeword being indicative of pixel intensity value represented by said first pixel codeword or as an instruction to invoke one or more image processing functions, and said processing unit operates to perform one or more image processing functions in response to said LUT codeword**.
> (Emphasis added.)

Claim 1, as amended, is patentable over the cited references at least by reciting "some of said pixel codewords being indicative of said pixel data and some of said pixel codewords having assigned values representing one or more image processing functions" and "said LUT

codeword being indicative of pixel intensity value represented by said first pixel codeword or as an instruction to invoke one or more image processing functions, and said processing unit operates to perform one or more image processing functions in response to said LUT codeword." In the claimed invention of claim 1, the pixel codewords stored in the data memory represent either pixel intensity values or have specially assigned values representing one or more image processing functions. Yamashita does not teach or suggest this limitation of claim 1 because Yamashita uses only RGB values which are converted to luminance signal Y and the luminance signal Y is processed by the correction coefficient calculation means 2 to generate a correction value K. Yamashita does not teach or suggest using pixel codewords that represent image processing functions. Furthermore, the correction coefficient calculation means 2 of Yamashita only calculates the correction value K and the correction value K is provided to multipliers 3, 4, 5 to simply multiply with the RGB signals. Yamashita does not teach or suggest using the output value from the correction coefficient calculation means to "invoke one or more image processing functions," as recited in claim 1.

For the above reasons, claim 1, as amended, is patentable over the cited references.

Claims 2 and 10-11

Claims 2 and 10-11, dependent upon claim 1, are patentable over the cited references at least for the same reasons claim 1 is patentable.

With respect to claim 10, the Examiner has taken official notice that it was well known at the time the invention was made to select an A/D conversion scheme from a plurality of possible schemes. Applicant hereby respectfully traverses the Examiner's assertion of official notice. ***Applicant submits that the factual assertion by the Examiner is not properly officially noticed and not properly based upon common knowledge***. In accordance with MPEP §2144.03, Applicant demands the Examiner to provide documentary evidence supporting the Official Notice in the next Office Action if the rejection is to be maintained. The error in the Examiner's action is as follows.

MPEP §2144.03 states that: "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known."

While official notice may be taken of a fact that is asserted to be "common knowledge" without specific reliance on documentary evidence, such official notice may be taken only where the fact noticed ***was readily verifiable*** or where there was nothing of record to contradict it. (See MPEP §2144.03.)

Both of the cited references are silent as to the provision of multiple A/D conversion schemes and selecting one of several A/D conversion schemes provided. Furthermore, Applicant's specification explained in paragraphs [0046] to [0047] that:

> **In a conventional digital image sensor, the image sensor has to be designed for a specific analog-to-digital conversion scheme**. However, the different ADC schemes are useful for different imaging conditions and thus the image sensor cannot be optimized for different types of usage. Also, the use and selection of a multi-capture scheme and a single capture scheme in an image sensor requires specific logic circuitry to be provided to handle the output data from the sensor array.
>
> However, in accordance with one embodiment of the present invention, **image sensor 100 can be programmed to implement any analog-to-digital conversion scheme or any single or multi-capture scheme without requiring change in hardware**…In this manner, **lookup table 116 enables the implementation of a variety of analog-to-digital conversion schemes** and enables the ready selection between a single capture or a multi-capture imaging scheme. (Emphasis added.)

Therefore, it is the inventors' contention that conventional image sensor uses only a single A/D conversion scheme and that additional scheme would require additional logic circuitry to implement. The image sensor of the present invention utilizes a lookup table to enable the implementation of a variety of analog-to-digital conversion schemes. If such implementation is indeed common knowledge, such a fact must be readily verifiable by the citing of a reference.

With respect to claim 11, the Examiner has taken official notice that using dark signal subtraction was well known at the time the invention was made. Applicant submits that while using dark signal subtraction itself may be well known, performing dark signal subtraction using the programmable lookup table and the processing unit in the manner as recited in claim 1 is not conventional.

§103 Rejection

Claims 12-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamashita in view of Post in further view of Fowler et al. (U.S. Patent No. 5,461,425). Claims 12-13, dependent upon claim 1, are patentable over Yamashita and Post for at least the same reasons claim 1 is patentable. Fowler does not cure the deficiency of Yamashita and Post. Therefore, claims 12-13 are patentable over all of the cited references.

CONCLUSION

For the reasons stated above, claims 1-24 are in condition for allowance and passage of the present case to allowance is respectfully requested. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

Certificate of Electronic Transmission

I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office using EFS-Web on the date shown below.

/Carmen C Cook/	October 3, 2007
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,

/Carmen C Cook/

Carmen C. Cook
Attorney for Applicant(s)
Reg. No. 42,433
Patent Law Group LLP
2635 N. First St.
Suite 223
San Jose, CA 95134
Tel (408) 382-0480 x208
Fax (408) 382-0481